WE CLAIM:

1. A method for forming an integrated circuit, comprising:

forming a magneto-resistive bit having an elongated central section and a first bit end, the first bit end having a perimeter and a width, the elongated central section having a width, the width of the first bit end being greater than the width of the elongated central section;

forming a dielectric layer adjacent to the first bit end; and

selectively removing a portion of the dielectric layer to form a hole, the hole having a perimeter and extending down to the magneto-resistive bit structure, wherein the hole is dimensioned such that the perimeter of the hole is spaced laterally inward of a perimeter of the first bit end.

2. The method of Claim 1, wherein the first dielectric layer comprises silicon nitride.

3. The method of Claim 1, wherein selectively removing comprises removing the portion of the dielectric layer using a preferential etch.

4. The method of Claim 1, wherein selectively removing comprises removing the portion of the dielectric layer using an anisotropic etch.

5. The method of Claim 1, wherein selectively removing comprises removing the portion of the dielectric layer using ion milling.

6. The method of Claim 1, wherein selectively removing comprises removing the portion of the dielectric layer using plasma etching.

7. The method of Claim 1, wherein selectively removing comprises:

providing a photoresist over the dielectric layer;

selectively applying light to areas where the dielectric layer is to be removed;

removing the photoresist to expose the portion of the dielectric layer that is to be removed; and

removing the exposed portion of the dielectric layer to form the hole.

8. The method of Claim 7, wherein removing the photoresist is accomplished using an oxygen asher photoresist strip.

9. The method of Claim 7, wherein selectively applying light is performed using electron beam photolithography.

10. The method of Claim 7, wherein selectively applying light includes applying ultraviolet (UV) light.

11. The method of Claim 1, further comprising:

forming a protective layer at least adjacent to the first bit end, prior to formation of the dielectric layer.

12. The method of Claim 11, wherein selectively removing comprises removing the dielectric layer to form the hole through the first dielectric layer, the hole extending down to the protective layer.

13. The method of Claim 11, wherein the protective layer is at least partially conductive.

14. The method of Claim 11, wherein the protective layer comprises chrome-silicon.

15. The method of Claim 1, wherein forming a magneto-resistive bit comprises forming a second bit end at an opposite end of the magneto-resistive bit from the first bit end, wherein the second bit end has a perimeter and a width.

16. The method of Claim 15, wherein the width of the second bit end is greater than the width of the elongated central section.

17. The method of Claim 15, wherein selectively removing comprises forming a second hole over the second bit end, wherein a perimeter of the second hole is spaced laterally inward of the perimeter of the second bit end.

18. The method of Claim 17, further comprising filling the second hole with one or more conductive materials, wherein filling the second hole forms a conductive contact with the second bit end.

19. The method of Claim 1, further comprising depositing a metal layer over the dielectric layer to at least partially fill the hole with metal.

20. The method of Claim 1, further comprising filling the hole with a low resistance material and then depositing a metal layer over the dielectric layer.

21. The method of Claim 20, wherein the low resistance material is tungsten.